FIG. 1

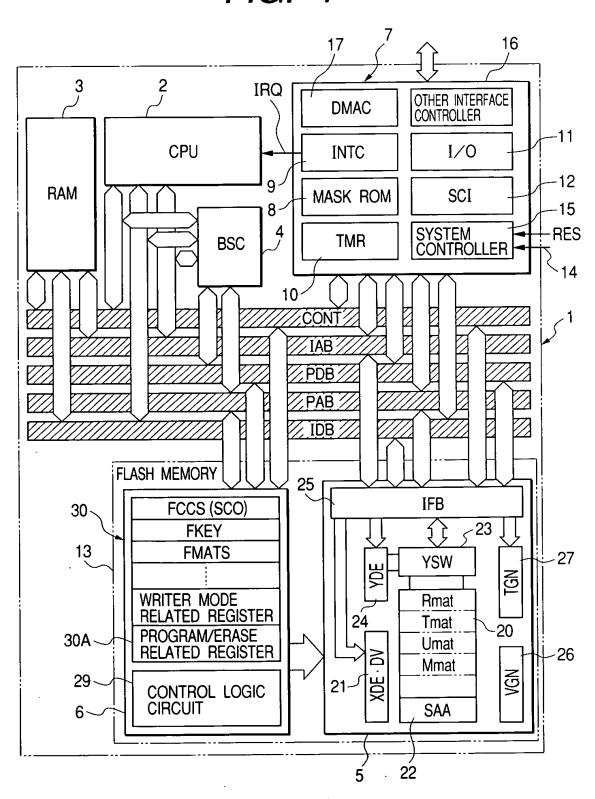


FIG. 2

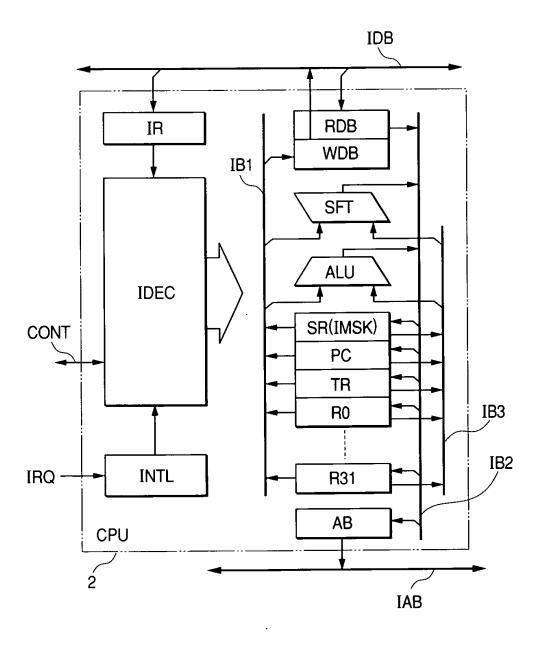


FIG. 3

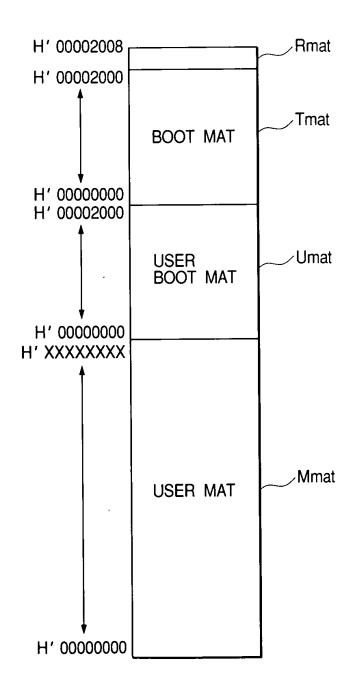
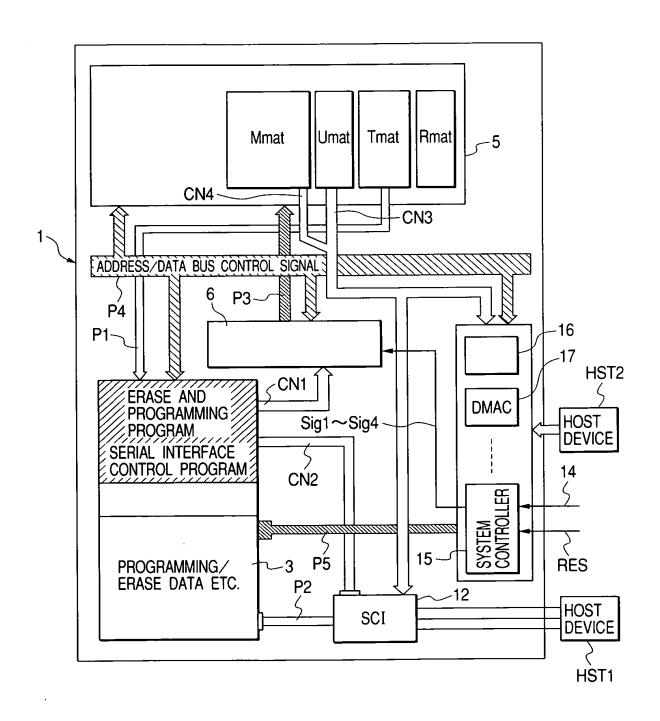


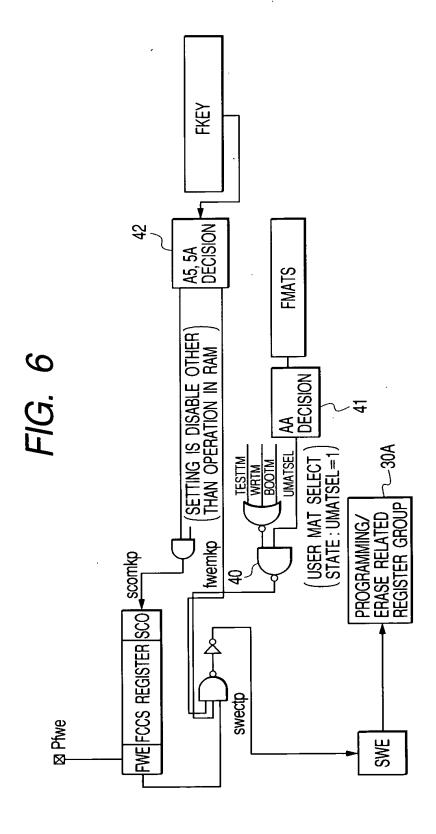
FIG. 4(A)

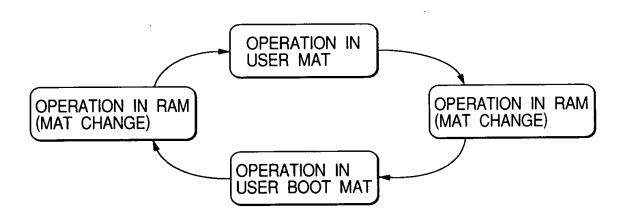
OPERATION MODE		BOOT MODE		A ·	WRITER MODE)E
MAT	ACCESS	PROGRAM	ERASE	ACCESS	ACCESS PROGRAM ERASE ACCESS PROGRAM	ERASE
USER MAT (Mmat)	0	0	0	0	0	0
USER BOOT MAT (Umat)	0	0	0	0	0	0
BOOT MAT (Tmat)	٥	×	×	V	×	×
REPAIR & TRIMMING (Rmat)	×	×	×	×	×	×

FIG. 4(B)

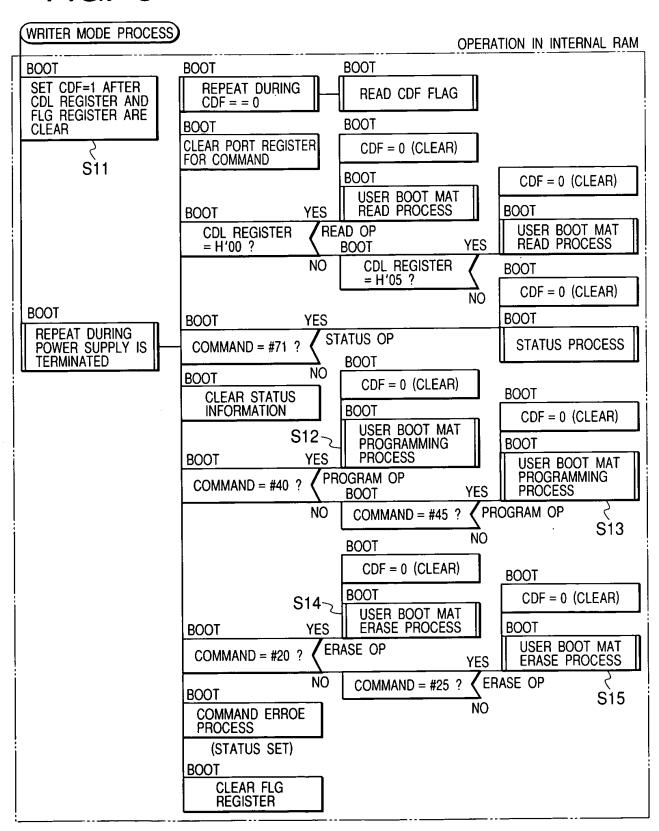
OPERATION MODE	ISN	USER BOOT MODE	ODE		USER MODE	
MAT	ACCESS	ACCESS PROGRAM	ERASE	ACCESS	ACCESS PROGRAM	ERASE
USER MAT (Mmat)	0	0	0	0	0	0
USER BOOT MAT (Umat)	0	×	×	0	×	×
BOOT MAT (Tmat)	∇	×	×	◁	×	×
REPAIR & TRIMMING (Rmat)	×	×	×	×	×	×

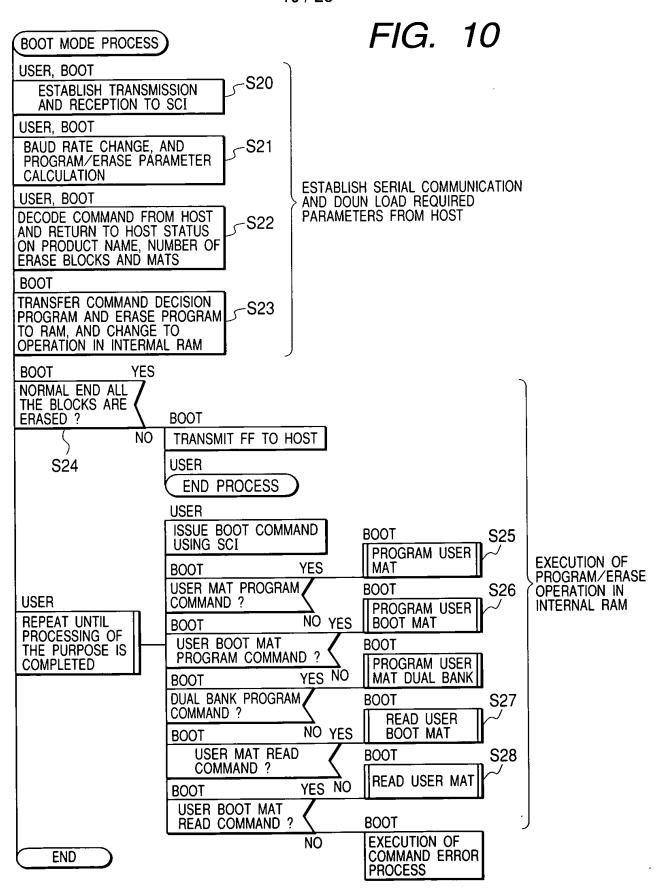


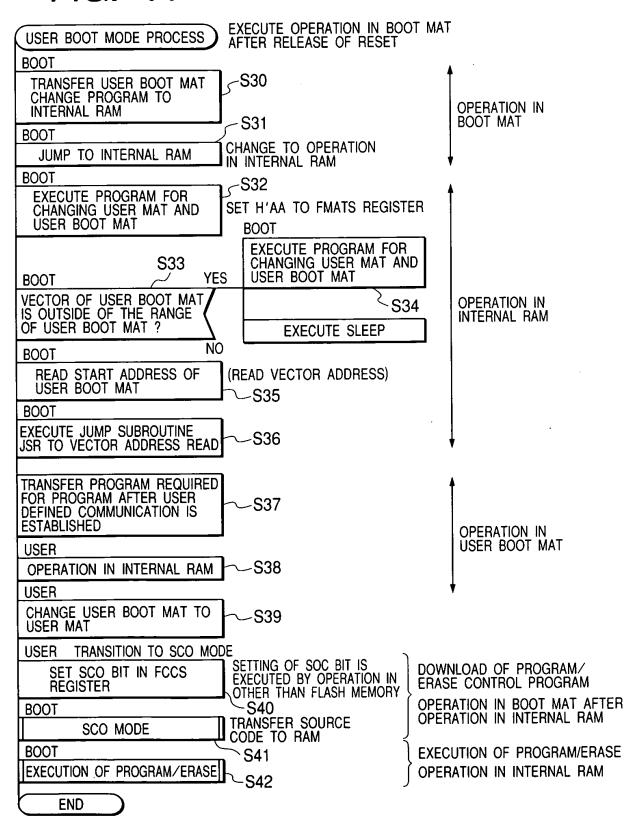


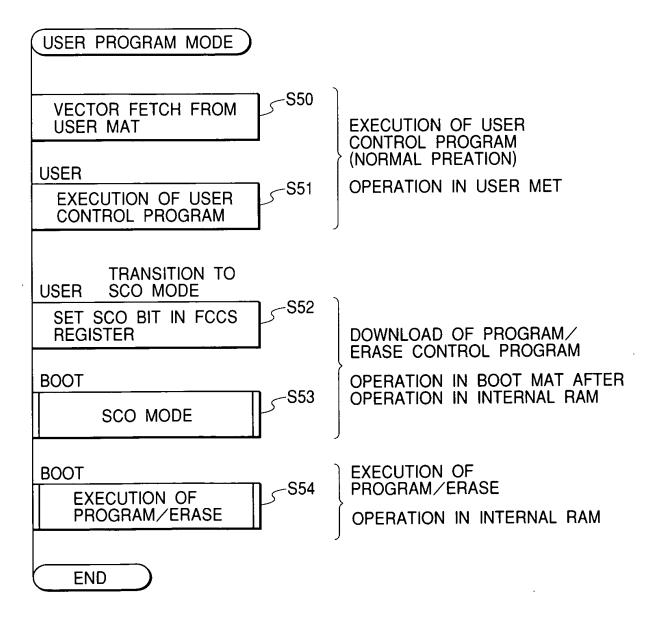


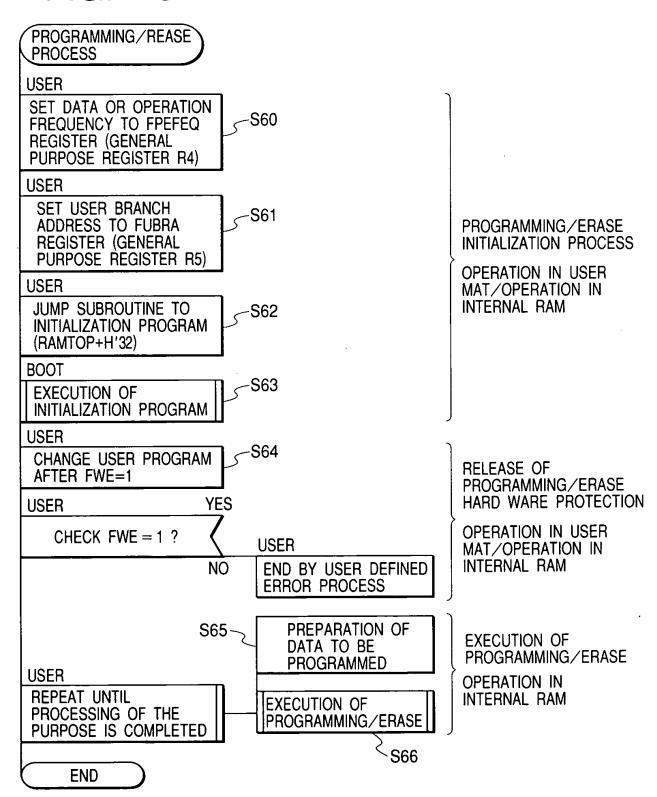
BOOT MODE USER	WRITER MODE	USER BOOT MODE USER	SCO MODE
RESET RELEASE AFTER SETTING MODE TERMINALS TO VOLTAGES FOR BOOT MODE	RESET RELEASE AFTER SETTING MODE TERMINALS TO VOLTAGES FOR WRITER MODE	RESET RELEASE AFTER SETTING MODE TERMINALS TO VOLTAGES FOR USER BOOT MODE	SET SCO-BIT IN INTERNAL PERIPHERAL REGISTER
CPU			OPERATION IN BOOT MAT
FETCH VECTOR FROM S' ADDRESS OF BOOT MAT	EXECUTION F ADDRESS IN	ROM USER BREAK BOOT MAT	BOOT WIAT
BOOT			-
STACK CONTENTS OF GENERAL PURPOSE REG	ISTERS		
READ MODE JUDGE #	CHANGE PROCESS FOR AFTER TRANSFERRING W	/RITE MODE	
REGISTER	CONTROL PROGRAM TO	INTERMAL RAM	
BOOT YES WRITER MODE ?	WRITER MODE	J	S3 S4
(WRTM=1) NO	BOOT MODE ?		TO PROCESS FOR
110	(BOOTM==1) NO	BOOT YES	SCO MODE
	TO PROCESS FOR	SCO MODE ? (SCO==1)	
BOOT YES USER BOOT MODE		~_ S5	
? (UBOOTM==1)	BOOT ERROR PROCESS		
BOOT RO	, ·		
FOR SCO MODE	Ρ		
EXECUTION OF PROCESS FOR BOOT MODE	J_S-87		
BOOT :	1		
EXECUTION OF PROCESS FOR WRITER MODE]_S8		
BOOT BOOCESS	1 ~S9		
EXECUTION OF PROCESS FOR USER BOOT MODE			
END			

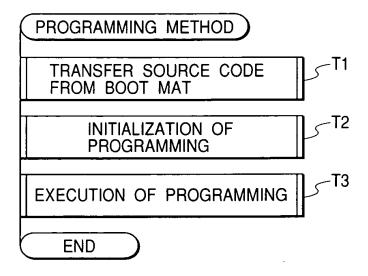


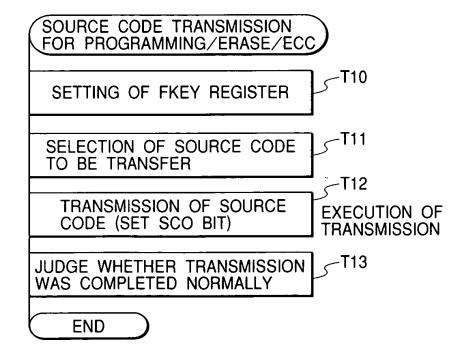


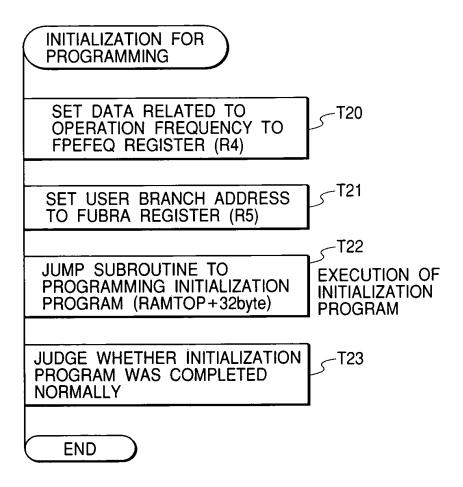












EXECUTION OF PROGRAMMING (PPVS, PPVD, ECPS)
CHANGE BRANCH ADDRESS FOR PROCESSING NMI TO ADDRESS OF INTERNAL RAM PLACE USER DEFINED ERROR PROCESSING ROUTINE TO INTERMAL RAM
INHIBIT INTERRUPT EXCEPT FOR T31 NMI USING SR REGISTER
SET SETTING AREA FOR WRITE ADDRESS TO R5
SET SETTING AREA FOR ADDRESS OF WRITE DATA TO R4
SET PROGRAM/ERASE CODE TO FKEY REGISTER
JUMP SUBROUTINE TO PROGRAMMING PROGRAM (RAMTOP+16byte) EXECUTION OF PROGRAMMING
T26
JUDGE WHETHER PROGRAMMING T36 WAS COMPLETED NORMALLY
END

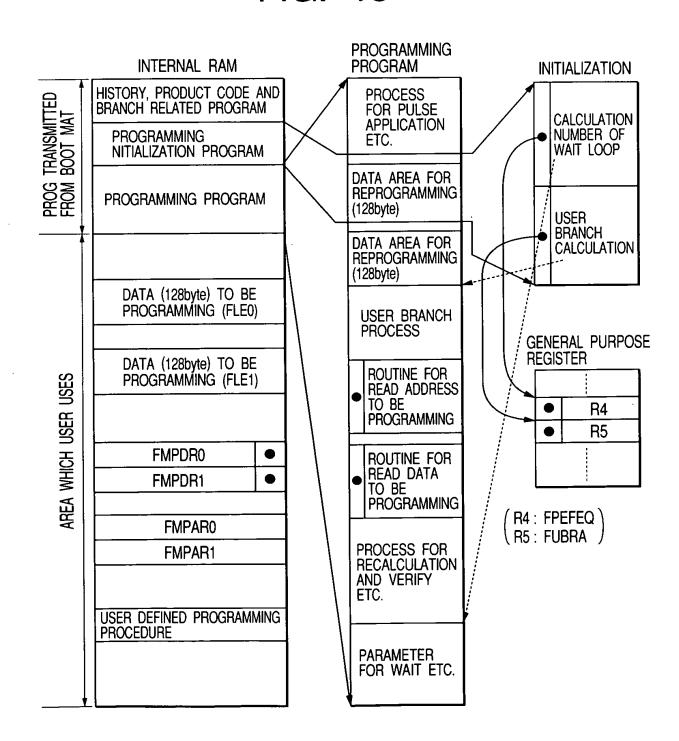
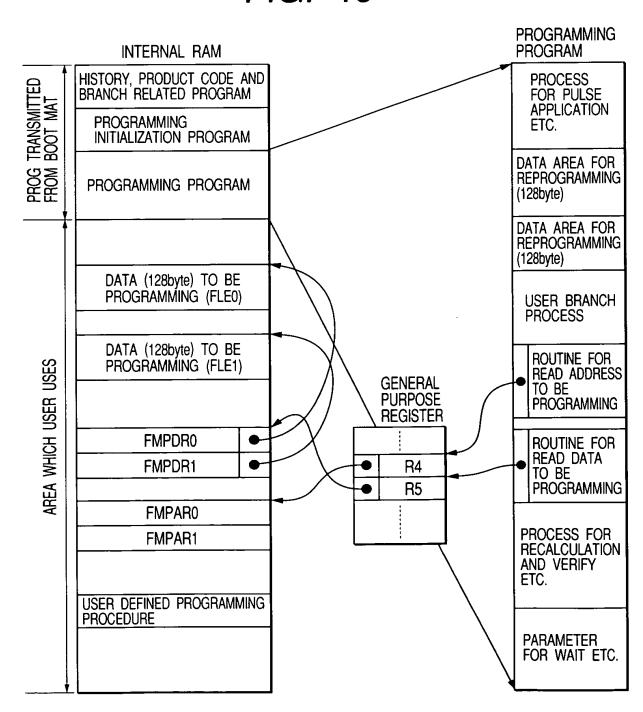
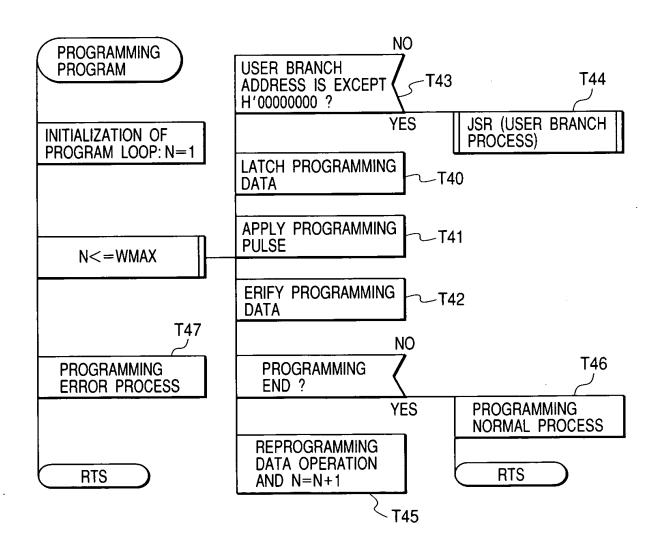
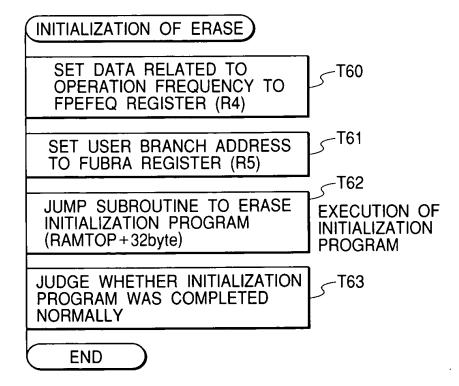


FIG. 19





ERASE METHOD	
TRANSMISSION OF SOURCE CODE FROM BOOT MAT	
EXECUTION OF INITIALIZATION	
EXECUTION OF REASE	- - - - - - - -
END	_



CHANGE BRANCH ADDRESS FOR PROCESSING NMI TO ADDRESS OF INTERNAL RAM INHIBIT INTERRUPT EXCEPT FOR NMI USING SR REGISTER SET ERASE BLOCK NUMBER TO R4 SET PROGRAM/ERASE CODE TO FKEY REGISTER T74 JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte) JUDGE WHETHER ERASE WAS COMPLETED NORMALLY END	
CHANGE BRANCH ADDRESS FOR PROCESSING NMI TO ADDRESS OF INTERNAL RAM INHIBIT INTERRUPT EXCEPT FOR NMI USING SR REGISTER SET ERASE BLOCK NUMBER TO R4 SET PROGRAM/ERASE CODE TO FKEY REGISTER T74 JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte) JUDGE WHETHER ERASE WAS COMPLETED NORMALLY	
CHANGE BRANCH ADDRESS FOR PROCESSING NMI TO ADDRESS OF INTERNAL RAM INHIBIT INTERRUPT EXCEPT FOR NMI USING SR REGISTER SET ERASE BLOCK NUMBER TO R4 SET PROGRAM/ERASE CODE TO FKEY REGISTER T74 JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte) JUDGE WHETHER ERASE WAS COMPLETED NORMALLY	
CHANGE BHANCH ADDRESS FOR PROCESSING NMI TO ADDRESS OF INTERNAL RAM INHIBIT INTERRUPT EXCEPT FOR NMI USING SR REGISTER SET ERASE BLOCK NUMBER TO R4 SET PROGRAM/ERASE CODE TO FKEY REGISTER TO FKEY REGISTER T74 JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte) JUDGE WHETHER ERASE WAS COMPLETED NORMALLY	\ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \ \
PROCESSING NMI TO ADDRESS OF INTERNAL RAM INHIBIT INTERRUPT EXCEPT FOR NMI USING SR REGISTER SET ERASE BLOCK NUMBER TO R4 SET PROGRAM/ERASE CODE TO FKEY REGISTER T72 JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte) JUDGE WHETHER ERASE WAS COMPLETED NORMALLY	CHANGE BRANCH ADDRESS FOR EDDOD DDOCESSING
INHIBIT INTERRUPT EXCEPT FOR NMI USING SR REGISTER SET ERASE BLOCK NUMBER TO R4 SET PROGRAM/ERASE CODE TO FKEY REGISTER TO FKEY REGISTER T74 JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte) JUDGE WHETHER ERASE WAS COMPLETED NORMALLY	PROCESSING NMI TO ADDRESS BOLITINE TO INTERMAL
SET ERASE BLOCK NUMBER TO R4 SET PROGRAM/ERASE CODE TO FKEY REGISTER T72 T73 JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte) JUDGE WHETHER ERASE WAS COMPLETED NORMALLY	OF INTERNAL RAM RAM
SET ERASE BLOCK NUMBER TO R4 SET PROGRAM/ERASE CODE TO FKEY REGISTER T72 T74 JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte) JUDGE WHETHER ERASE WAS COMPLETED NORMALLY	
SET ERASE BLOCK NUMBER TO R4 SET PROGRAM/ERASE CODE TO FKEY REGISTER T74 JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte) JUDGE WHETHER ERASE WAS COMPLETED NORMALLY	INHIBIT INTERHUPT EXCEPT FOR [>
SET PROGRAM/ERASE CODE TO FKEY REGISTER T74 JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte) JUDGE WHETHER ERASE WAS COMPLETED NORMALLY	NIVI USING SH REGISTER
SET PROGRAM/ERASE CODE TO FKEY REGISTER T74 JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte) JUDGE WHETHER ERASE WAS COMPLETED NORMALLY	257 50 405 PL 2014 NUMBER 1 772
SET PROGRAM/ERASE CODE TO FKEY REGISTER T74 JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte) SET PROGRAM/ERASE CODE T73 T74 EXECUTION OF ERASE JUDGE WHETHER ERASE WAS COMPLETED NORMALLY	SET ENASE BLOCK NOWIDER
JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte) JUDGE WHETHER ERASE WAS COMPLETED NORMALLY T74 EXECUTION OF ERASE T75	10 N4
JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte) JUDGE WHETHER ERASE WAS COMPLETED NORMALLY T74 EXECUTION OF ERASE T75	
JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte) STATE OF THE PROGRAM (RAMTOP+16byte) T74 EXECUTION OF ERASE T75 COMPLETED NORMALLY	SEI PHOGRAM/ ERASE CODE
JUMP SUBROUTINE TO ERASE PROGRAM (RAMTOP+16byte) EXECUTION OF ERASE JUDGE WHETHER ERASE WAS COMPLETED NORMALLY	
JUDGE WHETHER ERASE WAS COMPLETED NORMALLY	
JUDGE WHETHER ERASE WAS COMPLETED NORMALLY	DDOODAM (DAMTOD : 40b. 4-)
COMPLETED NORMALLY	FROGRAM (HAMITOT + TODYLE) ERASE
COMPLETED NORMALLY	
	1 JODGE WILLIAM ENAGE WAS 1
END	CONFLETED NORMALLY
(END)	5115
	END

en i,

FIG. 24

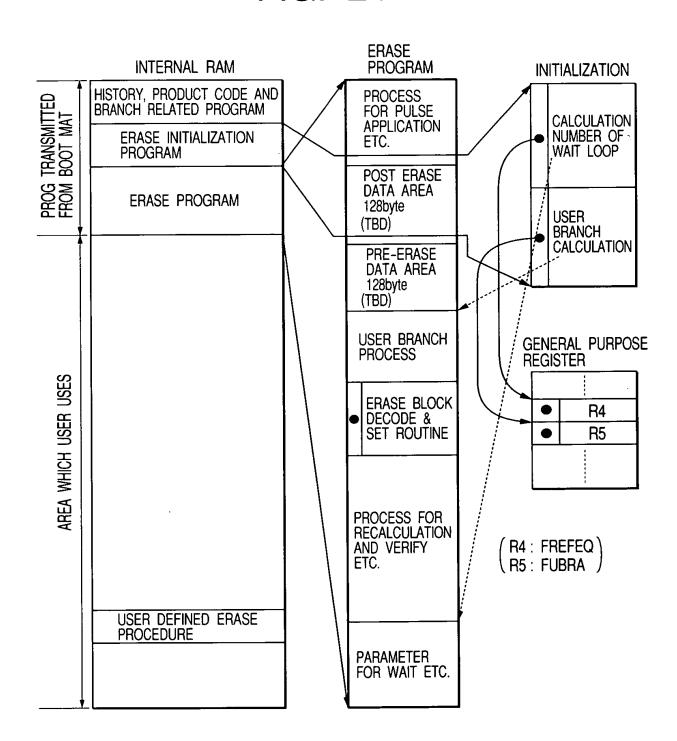


FIG. 25

